

Refine Search

Search Results -

Terms	Documents
(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	4

Database:

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L1

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<u>Set Name</u> <u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side		result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L1</u> (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	4	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	0

Database:

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L2

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<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L2</u>	(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	0	<u>L2</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L1</u>	(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	4	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
arbitration and (grant\$3 same concurrent same latenc\$3)	10

Database:

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Search:

L3

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Set Name Query

side by side

Hit Count Set Name

result set

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*L3 arbitration and (grant\$3 same concurrent same latenc\$3)10 L3*DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*L2 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)0 L2*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*L1 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)4 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
arbitration and (grant\$3 same concurrent same latenc\$3)	0

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L4

Refine Search

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side by side

Hit Count Set Name

result set

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4 arbitration and (grant\$3 same concurrent same latenc\$3)

 0 L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L3 arbitration and (grant\$3 same concurrent same latenc\$3)

 10 L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L2 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)

 0 L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L1 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)

 4 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(grant\$3 same concurrent same latenc\$3)	11

Database:

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Set Name Query

side by side

Hit Count Set Name

result set

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L5 (grant\$3 same concurrent same latenc\$3)

11 L5

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L4 arbitration and (grant\$3 same concurrent same latenc\$3)

0 L4

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 arbitration and (grant\$3 same concurrent same latenc\$3)

10 L3

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L2 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)

0 L2

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L1 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)

4 L1

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IEE JNL	IEE Journal or Magazine
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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

- ☐
- SAMBA-bus: A high performance bus architecture for system-on-chips**
Ruibing Lu; Cheng-Koh Koh;
Computer Aided Design, 2003. ICCAD-2003. International Conference on
9-13 Nov. 2003 Page(s):8 - 12
Digital Object Identifier 10.1109/ICCAD.2003.1257568
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SAMBA-bus: A high performance bus architecture for system-on-chips

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Abstract

A high performance communication architecture, SAMBA-bus, is proposed in this paper. In SAMBA-bus, multiple compatible bus transactions can be performed simultaneously with only a single bus access grant from the bus arbiter. Experimental results show that, compared with a traditional bus architecture, the SAMBA-bus architecture can have up to 3.5 times improvement in the effective bandwidth, and up to 15 times reduction in the average communication latency. In addition, the performance of SAMBA-bus architecture is affected only slightly by arbitration latency, because bus transactions can be performed without waiting for the bus access grant from the arbiter. This feature is desirable in SoC designs with large numbers of modules and long communication delay between modules and the bus arbiter.

Index Terms

Inspe

Controlled Indexing

asynchronous circuits circuit CAD system buses system-on-chip

Non-controlled Indexing

SAMBA bus architecture SOC design arbitration latency bus arbiter high performance bus architecture high performance communication architecture long communication delay multiple compatible bus transactions system-on-chip traditional bus architecture

Author Keywords

Not Available

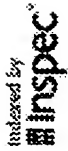
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